ABSTRACT OF THE DISCLOSURE

A line cache control system controls data flow between a line cache, a first central processing unit (CPU) and first and second memory devices. A first line cache interface that is associated with the first CPU receives a first program read request from the first CPU and generates a first address from the first program read request. A first memory interface communicates with the first memory device. A second memory interface communicates with the second memory device. A switch selectively connects a line cache to one of the first and second memory interfaces. When the line cache receives the first address, the line cache compares the first address to stored addresses in the line cache, returns data associated with the first address if a match occurs, and retrieves data from one of the first and second memory devices if a miss occurs.

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